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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/699,568	10/31/2003	Surya Varanasi	112-0132US	1585

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EXAMINER	
DUONG, FRANK	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/699,568	VARANASI ET AL.	
	Examiner	Art Unit	
	Frank Duong	2616	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 August 2005 and 31 October 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-158* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-158* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *31 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This Office Action is a response to communications dated 08/17/05 and 10/31/03. Claims 1-157 are presented in the application. It appears that claims 103-157 are misnumbered. The USPTO has applied 37 CFR 1.126 to renumber the claims to appear in a sequential order. Thus, claims 1-158 are pending in the application.

Information Disclosure Statement

2. The information disclosure statement filed 04/22/04 complies with the provisions of 37 CFR 1.97, 1.98 and MPEP § 609. It has been considered and placed in the application file.

Claim Objections

3. Claim 79-81 and 156 are objected to because of the following informalities:

As per claims 79-81, the claims appear to be improper dependent claims. In accordance with the claim language, claims 79-81 should be depended from claim 74 instead. They will be treated as such.

As per claim 156 (original claim 155), it is an improper dependent claim because it depends from itself.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 1-158 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

As per claims 1-32, the claims commonly recite the term "*so as to potentially reduce*," asserted to be indefinite.

As per claims 33-64, the claims commonly recite the terms "*is/are adapted to*" and "*so as to potentially reduce*," asserted to be indefinite. In addition, claims 41, 46, 51 and 56 also commonly recite the term "*as good as or better than*." This term further add ambiguities to the claims. In addition, claims 10, 14, 19 and 24 also commonly recite the term "*as good as or better than*." This term further adds ambiguities to the claims.

As per claims 65-96, the claims commonly recite the terms "is/are adapted to" and "*so as to potentially reduce*," asserted to be indefinite. In addition, claims 74, 78-80, 83, 85-86 and 88-90 also commonly recite the term "*as good as or better than*." This term further adds ambiguities to the claims.

As per claims 97-158, the claims are asserted to be indefinite for the same reasons discussed above.

A typical rationale for such assertions is that such language does not positively recite limitation that must be reasonably understood without resort to speculation. Thus, at least with respect to these recitations, the metes and bounds of the claims are essentially arguable and not determinable, and this situation yields the lack of adequate notice to a potential infringer.

Applicants are suggested to amend the claims to positively recite the claimed limitation and obviate the ambiguities discussed above.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1-9, 29-41, 61-79, 93-105, 125-135 and 153-157 are rejected under 35 U.S.C. 102(b) as being anticipated by Valdevit et al (Patent Application Publication US 2002/0156918) (hereinafter "Valdevit").

Regarding **claim 1**, in accordance with Valdevit reference entirety, Valdevit discloses a method of routing a flow of frames for a core-edge switch configuration (Figs. 1-6) comprising:

receiving at least one frame of said flow of frames at an edge switch of said configuration (*Fig. 6; block 602 and paragraph [0063]*);

applying a process to select a route from said edge switch to a core switch for said at least one frame of said flow of frames to reduce frame traffic congestion in said core-edge switch configuration (*Fig. 6; blocks 604-608 and paragraph [0063] and thereinafter*);

transmitting said at least one frame (*Fig. 6; block 610 and paragraph [0063]*).

Regarding **claim 2**, in addition to features recited in base claim 1 (see rationales discussed above), Valdevit also discloses wherein said process comprises a pseudo-random process (*see Fig. 6; block 606 or Abstract*).

Regarding **claim 3**, in addition to features recited in base claim 2 (see rationales discussed above), Valdevit also discloses wherein applying said pseudo-random process comprises applying a hash function (*see Fig. 6; block 606 or Abstract*).

Regarding **claim 4**, in addition to features recited in base claim 3 (see rationales discussed above), Valdevit also discloses wherein said hash function is also applied to a set of possible routes (*Fig. 2; routes 230 and 240*) to external exit ports (*Fig. 2; ports 226(3) and 226(4)*) of a core switch (*see Fig. 2 for detail connections of switched*) of said configuration to balance the flow of frames out said external exit ports *(see Fig. 6; block 608 and paragraph [0063] and Abstract*).

Regarding **claim 5**, in addition to features recited in base claim 3 (see rationales discussed above), Valdevit also discloses wherein said hash function is also applied to a set of possible routes to external exit ports of edge switches (*see Fig. 2 for detail connections of switched*) of said configuration to balance the flow of frames out said external exit ports *(see Fig. 6; block 608 and paragraph [0063] and Abstract*).

Regarding **claim 6**, in addition to features recited in base claim 3 (see rationales discussed above), Valdevit also discloses wherein said hash function is also applied to possible routes through said configuration to balance the flow of frames through said configuration to a particular external exit port of said configuration *(see Fig. 6; block 608 and paragraph [0063] and Abstract*).

Regarding **claim 7**, in addition to features recited in base claim 6 (see rationales discussed above), Valdevit also discloses wherein an external exit port of said configuration comprises an external exit port of an edge switch of said configuration (*see Fig. 2 for detail connections of switches*).

Regarding **claim 8**, in addition to features recited in base claim 3 (see rationales discussed above), Valdevit also discloses wherein said hash function is also applied to possible routes through said configuration to balance the flow of frames through said configuration to selected external exit ports of said configuration *(see Fig. 6; block 608 and paragraph [0063] and Abstract*).

Regarding **claim 9**, in addition to features recited in base claim 8 (see rationales discussed above), Valdevit also discloses wherein external exit ports of said configuration comprise external exit ports of edge switches of said configuration (*see Fig. 2 for detail connections of switches*).

Regarding **claim 29**, in addition to features recited in base claim 1 (see rationales discussed above), Valdevit also discloses wherein said route is selected based at least in part on a source tag and/or a destination tag added to said frame after said frame enters a switch of said core-edge switch configuration (Note: *Source and destination tags are discussed at paragraph [0063] and thereinafter).*

Regarding **claim 30**, in addition to features recited in base claim 29 (see rationales discussed above), Valdevit also discloses wherein said source tag and/or said destination tag is stripped off said frame before said frame exits said core switch

(Note: *Adding and removing source and destination tags are discussed at paragraph [0063] and thereinafter).*

Regarding **claim 31** in addition to features recited in base claim 29 (see rationales discussed above), Valdevit also discloses wherein said switch comprises a core switch (*see Fig. 2*).

Regarding **claim 32**, in addition to features recited in base claim 1 (see rationales discussed above), Valdevit also discloses wherein said switches of said configuration comprise fibre channel compliant switches (*see Fig. 2 and description of fibre channel compliant switches is discussed in the background and thereinafter*).

(*Note: Claims 33-41 and 61-64 call for an apparatus having limitations mirrored method steps of claims 1-9 and 29-32. Thus, they are rejected by the same rationales discussed above and as below*)

Regarding **claim 33**, in accordance with Valdevit reference entirety, Valdevit shows a switch fabric (*Fig. 1; 110*) comprising:

at least a first switch and a second switch (Fig. 2; 210-3,2 and 210-2,3 to 210-3,4), said first and said second switch being communicatively coupled (*Fig. 2; 230 and 240*);

said first switch (Fig. 4) including a processor (424 or 428) and memory (444);

said first switch selects a route for a frame of said flow of frames from an edge-switch to a core switch to reduce frame traffic congestion in a core-edge switch configuration (*Fig. 4 and paragraphs [0052] to [0054] or Fig. 6; blocks 604-610 and paragraph [0063] and thereinafter).*

Regarding **claim 34** in addition to features recited in base claim 33 (see rationales discussed above), Valdevit also discloses wherein said first switch pseudo-randomly selects a route for a frame of said flow of frames to reduce frame traffic congestion in said core-edge switch configuration (*Fig. 4 and paragraphs [0052] to [0054]).*

Regarding **claim 35** in addition to features recited in base claim 34 (see rationales discussed above), Valdevit also discloses wherein said first switch to pseudo-randomly selects a route by applying a hash function (*Fig. 6; block 608 and paragraph [0063] and thereinafter).*

Regarding **claim 36** in addition to features recited in base claim 35 (see rationales discussed above), Valdevit also discloses wherein said first switch also applies said hash function to a set of possible routes to external exit ports of a core switch of said configuration to balance the flow of frames out said external exit ports *(see Fig. 6; block 608 and paragraph [0063] and Abstract*).

Regarding **claim 37** in addition to features recited in base claim 35 (see rationales discussed above), Valdevit also discloses wherein said first switch is also adapted to apply said hash function to a set of possible routes to external exit ports of edge switches of said configuration to balance the flow of frames out said external exit ports *(see Fig. 6; block 608 and paragraph [0063] and Abstract*).

Regarding **claim 38** in addition to features recited in base claim 35 (see rationales discussed above), Valdevit also discloses wherein said first switch applies said hash function to possible routes through said configuration to balance the flow of

frames through said configuration to a particular external exit port of said configuration *(see Fig. 6; block 608 and paragraph [0063] and Abstract)*.

Regarding **claim 39** in addition to features recited in base claim 38 (see rationales discussed above), Valdevit also discloses wherein an external exit port of said configuration comprises an external exit port of an edge switch of said configuration (*see Fig. 2 for detail connections of switches*).

Regarding **claim 40** in addition to features recited in base claim 35 (see rationales discussed above), Valdevit also discloses wherein said first switch applies said hash function to possible routes through said configuration to balance the flow of frames through said configuration to selected external exit ports of said configuration *(see Fig. 6; block 608 and paragraph [0063] and Abstract)*.

Regarding **claim 41** in addition to features recited in base claim 40 (see rationales discussed above), Valdevit also discloses wherein external exit ports of said configuration comprise external exit ports of edge switches of said configuration (*see Fig. 2 for detail connections of switches*).

Regarding **claim 61** in addition to features recited in base claim 33 (see rationales discussed above), Valdevit also discloses wherein said first switch selects said route based at least in part on a source tag and/or a destination tag added to said frame after said frame enters a switch of said core-edge switch configuration (Note: *Source and destination tags are discussed at paragraph [0063] and thereinafter).*

Regarding **claim 62** in addition to features recited in base claim 61 (see rationales discussed above), Valdevit also discloses wherein said first switch strips said

source tag and/or said destination tag off said frame before said frame exits said first switch (Note: *Adding and removing source and destination tags are discussed beginning at paragraph [0063] and thereinafter).*

Regarding **claim 62** in addition to features recited in base claim 62 (see rationales discussed above), Valdevit also discloses wherein said first switch comprises a core switch (*see Fig. 2*).

Regarding **claim 63** in addition to features recited in base claim 62 (see rationales discussed above), Valdevit also discloses wherein said first switch comprises a fibre channel compliant switch (*see Fig. 2 and description of fibre channel compliant switches is discussed in the background and thereinafter*).

(*Note: The remaining claims call for an apparatus/methods having limitations variously relate to the above rejected claims. Thus, they are rejected by the same rationales discussed above and as below*)

Regarding **claim 65**, in accordance with Valdevit reference entirety, Valdevit shows an apparatus (Fig. 1; 110) comprising:

a switch (*Fig. 2; 210 or Fig. 4*), said switch (Fig. 4) including a processor (*424 and 428*) and memory (444);

said switch further having the capability to balance a flow of frames exiting said switch (paragraphs [0048]);

said switch selects a route for a frame of said flow of frames from an edge switch to a core switch to reduce frame traffic congestion in a core-edge switch configuration (*Fig. 6 and paragraph [0063] and thereinafter*).

Regarding **claim 66** in addition to features recited in base claim 65 (see rationales discussed above), Valdevit also discloses wherein said switch pseudo-randomly selects a route for a frame of said flow of frames to reduce frame traffic congestion in said core-edge switch configuration (*see Fig. 6; block 606 or Abstract*).

Regarding **claim 67** in addition to features recited in base claim 66 (see rationales discussed above), Valdevit also discloses wherein said switch pseudo-randomly selects a route by applying a hash function (*see Fig. 6; block 606 or Abstract*).

Regarding **claim 68** in addition to features recited in base claim 67 (see rationales discussed above), Valdevit also discloses wherein said switch applies said hash function to a set of possible routes to external exit ports of a core switch of said configuration to balance the flow of frames out said external exit ports (*see Fig. 6; blocks 606-610 or Abstract*).

Regarding **claim 69** in addition to features recited in base claim 67 (see rationales discussed above), Valdevit also discloses wherein said switch applies said hash function to a set of possible routes to external exit ports of edge switches of said configuration to balance the flow of frames out said external exit ports (*see Fig. 6; blocks 606-610 or Abstract*).

Regarding **claim 70** in addition to features recited in base claim 67 (see rationales discussed above), Valdevit also discloses wherein said switch applies said hash function to possible routes through said configuration to balance the flow of frames

through said configuration to a particular external exit port of said configuration (*see Fig. 6; blocks 606-610 or Abstract*).

Regarding **claim 71** in addition to features recited in base claim 70 (see rationales discussed above), Valdevit also discloses wherein an external exit port of said configuration comprises an external exit port of an edge switch of said configuration (*see Fig. 2 for connection details*).

Regarding **claim 72** in addition to features recited in base claim 67 (see rationales discussed above), Valdevit also discloses wherein said switch applies said hash function to possible routes through said configuration to balance the flow of frames through said configuration to selected external exit ports of said configuration (*see Fig. 6; blocks 606-610 or Abstract*).

Regarding **claim 73** in addition to features recited in base claim 72 (see rationales discussed above), Valdevit also discloses wherein external exit ports of said configuration comprise external exit ports of edge switches of said configuration (*see Fig. 2 for connection details*).

Regarding **claim 93** in addition to features recited in base claim 65 (see rationales discussed above), Valdevit also discloses wherein said switch selects said route based at least in part on a source tag and/or a destination tag added to said frame after said frame enters a switch of said core-edge switch configuration (Note: *Source and destination tags are discussed beginning at paragraph [0063] and thereinafter).*

Regarding **claim 94** in addition to features recited in base claim 93 (see rationales discussed above), Valdevit also discloses wherein said switch strips said source tag and/or said destination tag off said frame before said frame exits said switch (Note: *Adding and removing source and destination tags are discussed beginning at paragraph [0063] and thereinafter).*

Regarding **claim 95** in addition to features recited in base claim 65 (see rationales discussed above), Valdevit also discloses wherein said switch comprises a fibre channel compliant switch (*see Fig. 2 and description of fibre channel compliant switches is discussed in the background and thereinafter*).

Regarding **claim 96** in addition to features recited in base claim 65 (see rationales discussed above), Valdevit also discloses wherein said switch comprises a core switch of said core-edge switch configuration (*see Fig. 2*).

Regarding **claim 97**, in accordance with Valdevit reference entirety, Valdevit shows a network (Fig. 2) comprising:

a host (*Fig. 2 depicts details of switch fabric having a host (source or destination)*));

a physical storage unit (*Fig. 2 depicts details of switch fabric connecting to other elements to include storage unit 136*);

a first switch (210-3,2) and a second switch (210-3,4) communicatively coupled to form a switch fabric (see *Fig. 2 for connection details*);

said first switch and said second switch further communicatively coupled (230 and 240) to said host (source or destination) and said physical storage unit (136) (see Fig. 2 for connection details);

said first switch at least including a processor and memory (*see Fig. 4 for details of individual switch having processor ((424 or 428) and memory 444*);

said first switch selects a route for a frame of said flow of frames from an edge switch to a core switch to reduce frame traffic congestion in a core-edge switch configuration (*the route selection process for routing a frame is depicted in Fig. 6 and accompanied description starting from paragraph [0063] and thereinafter*).

Regarding **claim 98** in addition to features recited in base claim 97 (see rationales discussed above), Valdevit also discloses wherein said first switch pseudo-randomly selects a route for a frame of said flow of frames to reduce frame traffic congestion in said core-edge switch configuration (see paragraph [0055] and thereinafter).

Regarding **claim 99** in addition to features recited in base claim 98 (see rationales discussed above), Valdevit also discloses wherein said first switch pseudo-randomly selects a route by applying a hash function (see paragraph [0063] and thereinafter).

Regarding **claim 100** in addition to features recited in base claim 99 (see rationales discussed above), Valdevit also discloses wherein said first switch applies said hash function to a set of possible routes to external exit ports of a core switch of

said configuration to balance the flow of frames out said external exit ports (see paragraph [0063] and thereinafter).

Regarding **claim 101** in addition to features recited in base claim 99 (see rationales discussed above), Valdevit also discloses wherein said first switch applies said hash function to a set of possible routes to external exit ports of edge switches of said configuration to balance the flow of frames out said external exit ports (see paragraph [0063] and thereinafter).

Regarding **claim 102** in addition to features recited in base claim 99 (see rationales discussed above), Valdevit also discloses wherein said first switch applies said hash function to possible routes through said configuration to balance the flow of frames through said configuration to a particular external exit port of said configuration (see paragraph [0063] and thereinafter).

Regarding **claim 103** in addition to features recited in base claim 102 (see rationales discussed above), Valdevit also discloses wherein an external exit port of said configuration comprises an external exit port of an edge switch of said configuration (see Fig. 2 for detail connections of switch fabric to include ports).

Regarding **claim 104** in addition to features recited in base claim 99 (see rationales discussed above), Valdevit also discloses wherein said first switch applies said hash function to possible routes through said configuration to balance the flow of frames through said configuration to selected external exit ports of said configuration (see paragraph [0063] and thereinafter).

Regarding **claim 105** in addition to features recited in base claim 104 (see rationales discussed above), Valdevit also discloses wherein external exit ports of said configuration comprise external exit ports of edge switches of said configuration (see Fig. 2 for detail connections of switch fabric to include ports).

Regarding **claim 125** in addition to features recited in base claim 97 (see rationales discussed above), Valdevit also discloses wherein said first switch selects said route based at least in part on a source tag and/or a destination tag added to said frame after said frame enters a switch of said core-edge switch configuration (Note: *Adding and removing source and destination tags are discussed beginning at paragraph [0063] and thereinafter).*

Regarding **claim 126** in addition to features recited in base claim 97 (see rationales discussed above), Valdevit also discloses wherein said first switch strips said source tag and/or said destination tag off said frame before said frame exits said first switch (Note: *Adding and removing source and destination tags are discussed beginning at paragraph [0063] and thereinafter).*

As per **claims 127-135 and 153-154**, the claims call for an article having limitations mirrored that of claims 97-105 and 125-126. Thus, they are anticipated by the same rationales discussed above.

As per **claims 155-157**, the claims call for an article having limitations mirrored that of claims 97-99. Thus, they are anticipated by the same rationales discussed above.

Double Patenting

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

6. Claims 1-158 are provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1-95 of copending Application No. 10/698,851. Although the conflicting claims are not identical, they are not patentably distinct from each other because of the following rationales:

Claim 1 of the instant application is a representative claim and it calls for:

A method of routing a flow of frames for ***a core-edge switch configuration*** comprising:

receiving at least one frame of said flow of frames ***at an edge switch of said configuration***;

applying a process to select ***a route from said edge switch*** to a core switch for said at least one frame of said flow of frames so as to potentially reduce frame traffic congestion in said core-edge switch configuration;

transmitting said at least one frame.

Claim 1 of the '851 copending application is a representative claim and it calls for:

A method of routing a flow of frames through ***a switch*** comprising:

receiving at least one frame from said flow of frames;

applying a process to select ***an exit port of said switch*** from a set of possible exit ports through which at least one frame from said flow of frames will exit so as to potentially reduce frame traffic congestion **along potential routes** that include said set of possible exit ports, said set of possible exit ports ***including at least some of the exit ports of at least two trunk groups***;

transmitting said at least one frame.

A careful review of the claimed inventions one could clearly see that the claimed limitations of the instant application is a broader version of the '851 copending application. However, there is a difference between the claimed inventions depicted in the bolded words. Such difference relates to the language usage or omitting limitation and it's deemed to be obvious or field expedient by a skilled artisan.

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

7. Claims 10-28, 42-60, 74-92, 106-124, 136-152 and 158 provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 12, 35, 52, 72 or 92 of copending Application No. 10/699,567 in view of Valdevit.

Claims 12, 35, 52 72 or 92 of the '567 copending application claims applying weights to select particular port of said switch as an egress port for a particular frame of said frames exiting the switch, said particular port being selected from among available ports of said switch. Claims 12, 35, 52 72 or 92 of the '567 copending application may not explicit recite the limitations of receiving a frame, applying a hash function to select a route to reduce traffic congestion and transmitting the frame. However, such limitations lack thereof from copending application are well known and taught by Valdevit.

As discussed in the 102(b) rejection section above, Valdevit teaches the missing limitation in a manner as claimed. Thus, it would have been obvious to those skilled in the art at the time of the invention to incorporate Valdevit's teaching into the '567 copending application to arrive the claimed invention with a motivation to alleviate traffic congestion (Valdevit; paragraph [0011]).

This is a provisional obviousness-type double patenting rejection.

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Examiner reserve the right to apply the below references in a subsequent Office Action.

Soloway et al (USP 6,532,212).

Luke et al (USP 6,985,956).

Lay et al (USP 6,862,293).

Edsall et al (USP 5,742,604).

Valdevit, Fabric Shortest Path First (FSPF) Revision 0.1, Brodecade, pages 1-10, March 2000.

Tech Node, Exploring Brodecade ISL Trunking, Brodecade, pages 1-26, January 2002.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Frank Duong whose telephone number is 571-272-3164. The examiner can normally be reached on 7:00AM-3:30PM, Monday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynn D. Feild can be reached on 571-272-2092. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

FRANK DUONG
PRIMARY EXAMINER

July 8, 2007